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ECE 164 Project

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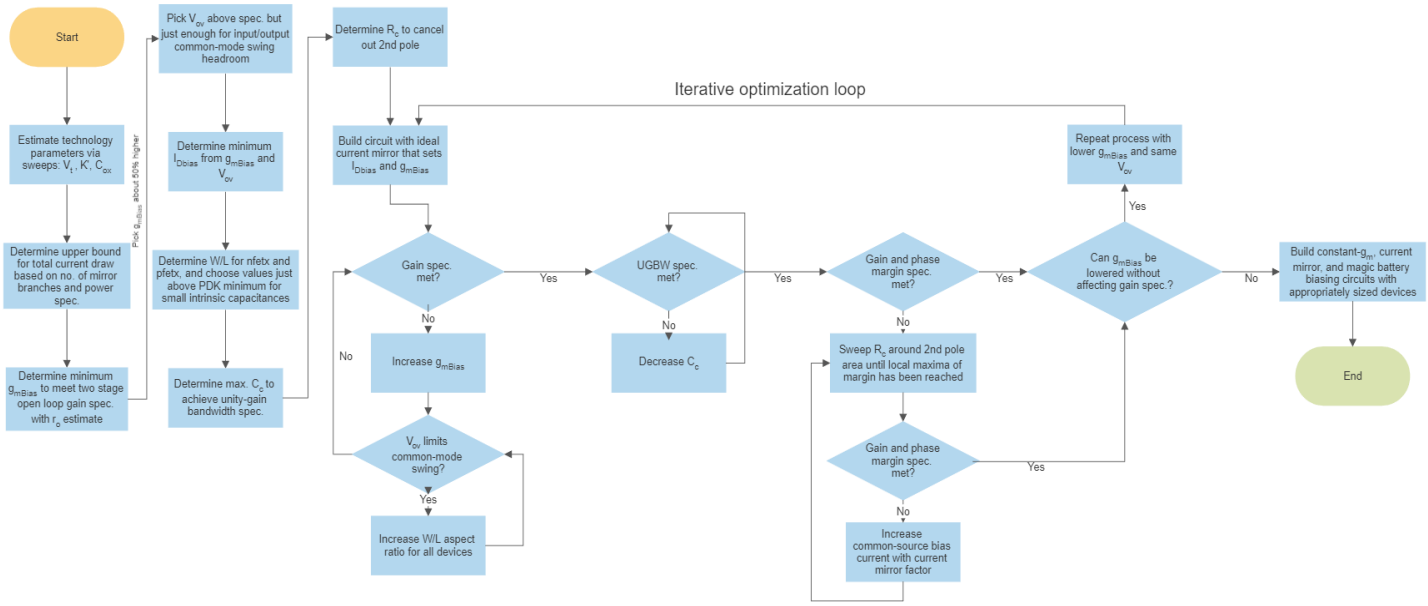
Design Strategy

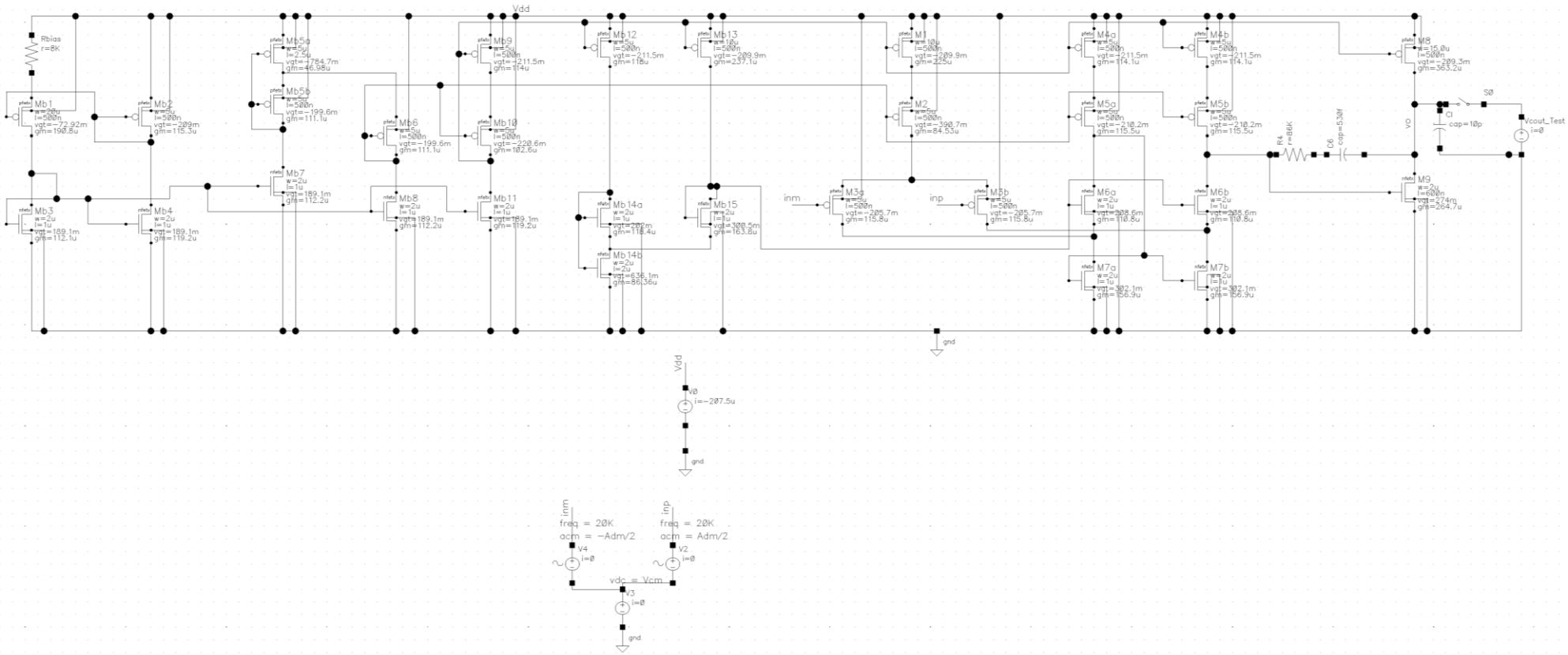


Starting out, it was clear that there were a lot of "knobs" to tweak – my strategy was to reduce the variable count by fixing parameters V_{ov}, I_{DBias}, and g_{mBias} to values informed by the total gain and power specification. Therefore, it is illustrated in the design flow chart that by having a nominal value for these variables, transistor sizing and compensation resistance and capacitance values can be estimated from hand calculations. It is worth noting that r_o's nominal value was crucial to gain calculations – since this is linked to lambda which varies depending on context, r_o had to be estimated based on past encounters in simulation of the same technology. However, r_o need not be accurate, only within a reasonable order of magnitude, since we can tweak gain with g_{mBias}. The latter half of my strategy goes through each spec. and presents a somewhat decoupled parameter to change i.e. in other words, the change related to one spec. should not affect a spec. that came before; the change of a spec. can also enhance the one before. For example, a decrease of C_c does not decrease DC gain, nor does the sweep of R_c.

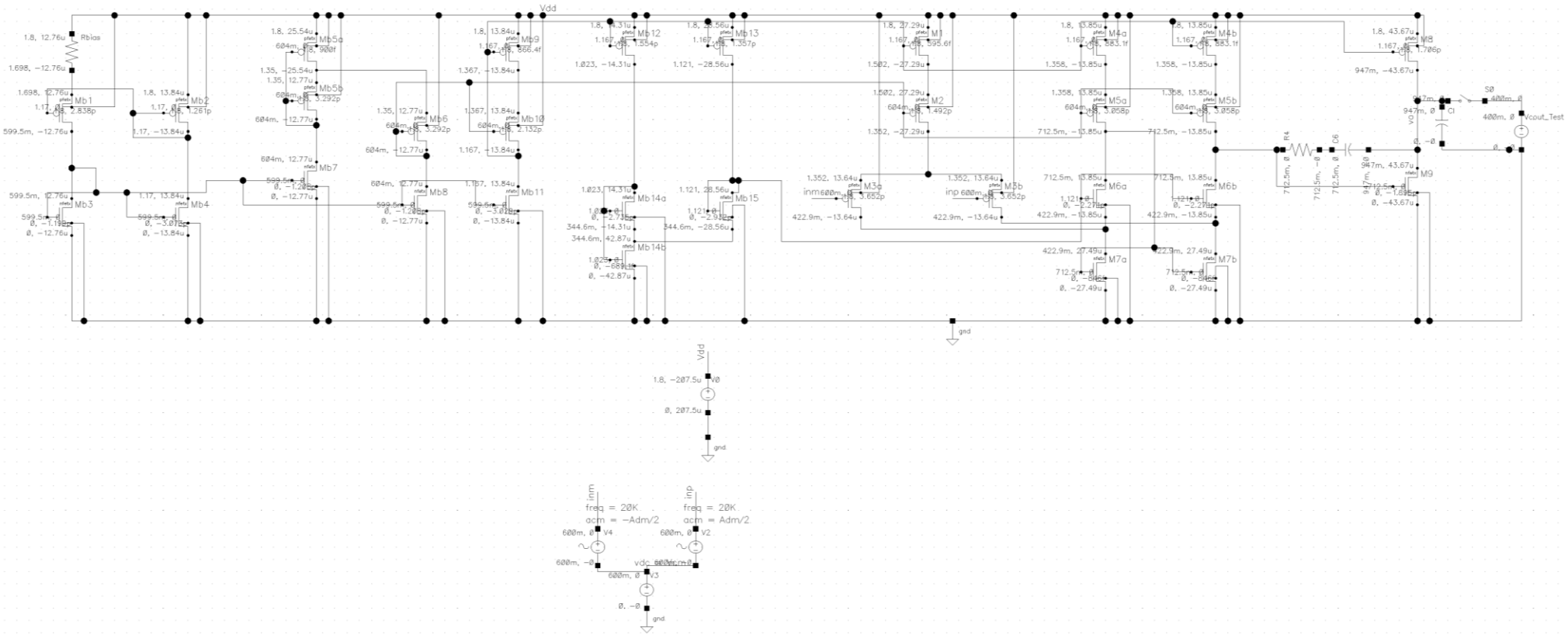
Once a circuit with ideal biasing complies with specs., we begin the second optimization iteration by decreasing g_{mBias}, going through the same process of spec. meeting. By keeping V_{ov} fixed to preserve swing range, I_{Dbias} must also decrease, and thus power. The idea is that by the first iteration, component values should already be within the ballpark of an optimum, and each iteration thereafter should match specs with lower power. We stop optimizing when current is low to achieve gain spec.

The last step is to convert the ideal bias network to a constant-g_m, current mirror, and magic battery circuits, with appropriate sizing to achieve proper bias voltages for maximum common-mode swing and saturation operation.

Component values, overdrive voltages, transconductances



DC voltages and currents



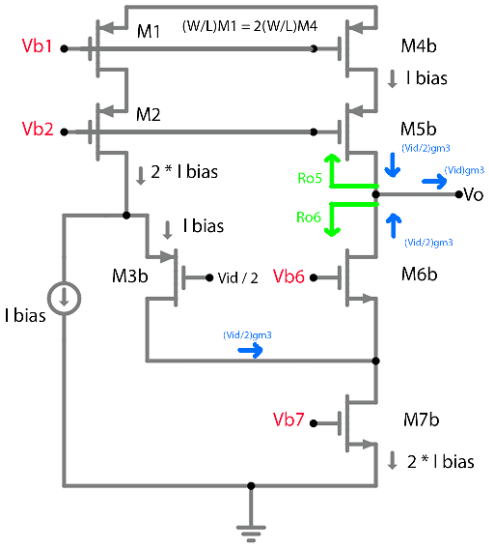
Design Parameters Calculations

Technology parameters

Before any hand calculations take place, some technology parameters must be acquired via simulation sweeping – these values will deviate in the final simulation due to many factors such as changes in sizing and the body effect, however the hand calculations still should be within range of simulated values. From homework 1, V_{ton}, V_{top}, K'_n, and K'_p were found by sweeping L and finding the slope and y-intercept of I_{DS} vs. L for the transistors in saturation for threshold voltage and triode for K'.
V_{otp} = 0.38V, but we can round to 0.4V for simplicity and to generally account for the body effect. Similarly, V_{ton} = 0.307V is rounded to 0.32V.
K'_p = 49.1µA/V^2 rounded to 50. K'_n = 267.2µA/V^2 rounded to 270.
C_{ox} was found in homework 3 by sweeping L and observing a triode transistor's C_{gg} value in simulation which makes up both C_{gs} and C_{gd} which are approximately equal.
C_{ox} = 7.33fF/µm^2

Gain

From the half-circuit of the folded cascode, we can observe that the output current is $V_{id}g_{m3}$, thus the gain is approximately:



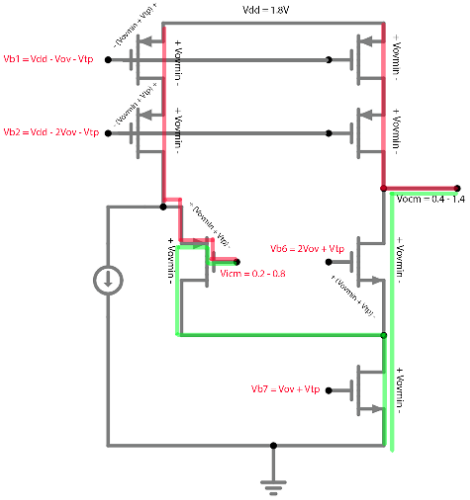
$A_{v1} = g_{m3} R_o = g_{m3} (R_{o5} \parallel R_{o6})$ where:
$R_{o5} = g_{m5b} r_{o5b} r_{o5a} = g_{mBias} r_o^2$
$R_{o6} = g_{m6b} r_{o6b} (R_{o3} \parallel R_{o7}) = g_{mBias} r_{o6b} (r_{o3b} \parallel r_{o7b})$

r_o as previously explained varies based on higher order factors. For simplicity, r_o for devices in saturation is said to be approximately 1MΩ. On the other hand, devices that are in triode region significantly drop in resistance, to around 1/100th of that, or 10kΩ. These estimated values should be easy to correct once simulation shows the actual operating points. From these values, the expected gain from the folded cascode stage is:
$g_{mBias} ((g_{mBias} * 10^{12}) \parallel (g_{mBias} * 10^6 * 10000)) = 10^{10} g_{mBias}^2$
In general, g_{mBias} is a knob for gain; high gain trades off power consumption.
Similar analysis can be done for the gain of the common-source second stage, which is approximately:
$A_{v2} = g_{m9} R_o = g_{m9} (r_{o9} \parallel r_{o8})$. If we assume that r_{o8} and r_{o9} are equal:
$A_{v2} = 0.5\ g_{m9}\ r_o = 500k\ g_{m9}$
It is clear that the second stage is controlled by g_{m9}, which is determined by I_{D9}, controlled by the PMOS current mirror multiplier K of $(KW/L)_{M8}$.

The total open loop gain is:
$A_v = A_{v1} A_{v2} = 1M * 500k * g_{mBias}^2$
For a total open loop gain of 70db, this is equivalent to 3163 of voltage gain. If we assume g_{m9} is g_{mBias} – in the words the current multiplier is 1, g_{mBias} would have to be approximately 86 µS. Going through the iterative optimization loop, g_{mBias} converged towards a value of approximately 100 µS – this would yield a gain of 73.9dB.

V_{ov}

A small V_{ov} is desirable as it allows more input and output swing for both amplifier stages i.e. V_{DS} of the devices that are affected by swing can be decreased more while maintaining saturation conditions. However, since the spec. sets a floor of 0.15V, we want to stick as close to that value as possible while giving some room for fluctuation due to non-idealities. For example, since $V_{ov} = (2 I_D / K' W/L)^{0.5}$, V_{ov} fluctuations can only be caused by I_D fluctuations given that all other variables are fixed – this is a likely occurrence because of mismatch of current mirrors i.e. hand calculated I_D will not match simulation. Overall, a standardized $V_{ov} = 0.2V$ mitigates spec. violation in the case of I_D variations.



Common-mode input / output range

With a V_{ov} of 0.2V set, both common input and output ranges will be met where no transistors will go out of saturation. This is illustrated below by tracing the limiting signal paths to either GND or V_{DD}. Additionally, gate bias voltages, in terms of V_{ov} and V_t, can be set by magic batteries to ensure maximum headroom.

I_{DBias}

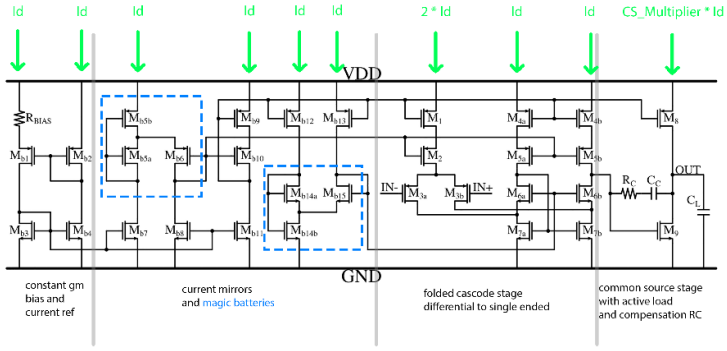
Since we require a g_{mBias} of at least 100µS to reach the gain spec. and we have decided on a V_{ov}, this determines I_{DBias}:
$I_{DBias} = (V_{ov} g_{mBias}) / 2 = 10$ µA

W/L

$(W/L)_p = 2 I_{DBias} / (K'_p * V_{ov}^2) = 10$
$(W/L)_n = 2 I_{DBias} / (K'_n * V_{ov}^2) = 1.87$ rounded to 2
W should not be set too high due to intrinsic capacitances being dominant, however should be large enough to avoid the PDK length minimum and allowing W to vary as DC operating points shift. W_n is set to 2µ, and W_p is set to 5µ.

Power

Power can be calculated via:
$P_{total} = I_{total} * V_{DD}$
The total current draw is the sum of current draw from each branch, a multiple of I_{DBias}. From the diagram, the total current must be at least 11 I_{DBias}, assuming the CS stage only draws I_{DBias}, for all bias circuits to work and the gain spec. to be met.
$P_{min} = 11 * I_{DBias} * V_{DD} = 0.198$ mW



Frequency response

By adding $C_c = 530$ fF, we've introduced one dominant LHP pole, one non-dominant LHP pole, and one RHP zero:
$f_{p1} = 1 / (C_c\, g_{m9}\, (r_{o8} \,||\, r_{o9})\, R_{o1}\, 2\pi)$, we know R_{o1} from calculations of folded-cascode gain. Since r_o is assumed to be 1MΩ:
$f_{p1} = 1 / (C_c\, g_{mBias} * 500k * 1M * 2\pi) = 6006$ Hz
$f_{p2} = g_{m9} / (C_{GS9} + C_{Load})\, 2\pi = g_{mBias} / C_{Load}\, 2\pi = 1.59$ MHz, assuming
$C_{GS9} = 2/3\ W\ L\ C_{ox} << C_{Load}$
$f_Z = g_{m9} / C_c\, 2\pi = g_{mBias} / C_c\, 2\pi = 30.02$ MHz = UGBW
Since the zero is expect to fall at the UGBW, there is no worry at it degrading this metric since the gain will experience a +20dB/dec slope.
The poles are relatively close to each other which is not great for phase margin. Nulling resistor R_c can be added to place a zero at P_2 cancel it out and maintain a -20dB slope:
$R_c = C_c + C_{Load} / (C_c\, g_{m9}) = 200$kΩ
R_c's final value will deviate (or luckily not) from this depending on the actual placement of the 2nd pole, and the actual margin performance. The design flow accounts for this, and allows R_c to be swept for optimal margins.

Biasing circuits

Constant-g_m bias circuit allows gm for all mirroring PMOS to be set, assuming that $(W/L)_{Mb1} / (W/L)_{Mb2} = 4$:
$g_{mBias} = 1 / R_{Bias}$, thus g_{mBias} of 100μS would require $R_{Bias} = 10$kΩ
To set I_{DBias} with given R_{Bias}:
$I_{DBias} = 1 / (K'p * (W/L)_{Mb2} * 2 * R_{Bias}^2) = 10$μA, thus $(W/L)_{Mb2} = 10$

Magic battery M_{b5a} and M_{b5b} is used to bias M_2 to $V_{DD} - 2V_{ov} - V_{tp}$, approximately 0.7V. Since M_{b5a} is receiving $2I_{DBias}$, V_{ov} increases to 0.28V. The voltage drop from V_{DD}, and ultimately the bias voltage VB is:

$V_B = V_{DD} - (K + 1)^{0.5}\, V_{ov} + V_{tp} = 0.71$V assuming M_{b5a} is 6 times smaller than M_{b5b}.

Similarly, M_{6a} and M_{6b} are biased by battery M_{b14a} and M_{b14b} to roughly $2V_{ov} + V_{tn}$, thus Mb14a is twice as large.

The following table outlines the differences between calculated and simulated relevant parameters. Orange highlight indicates some significant deviation.

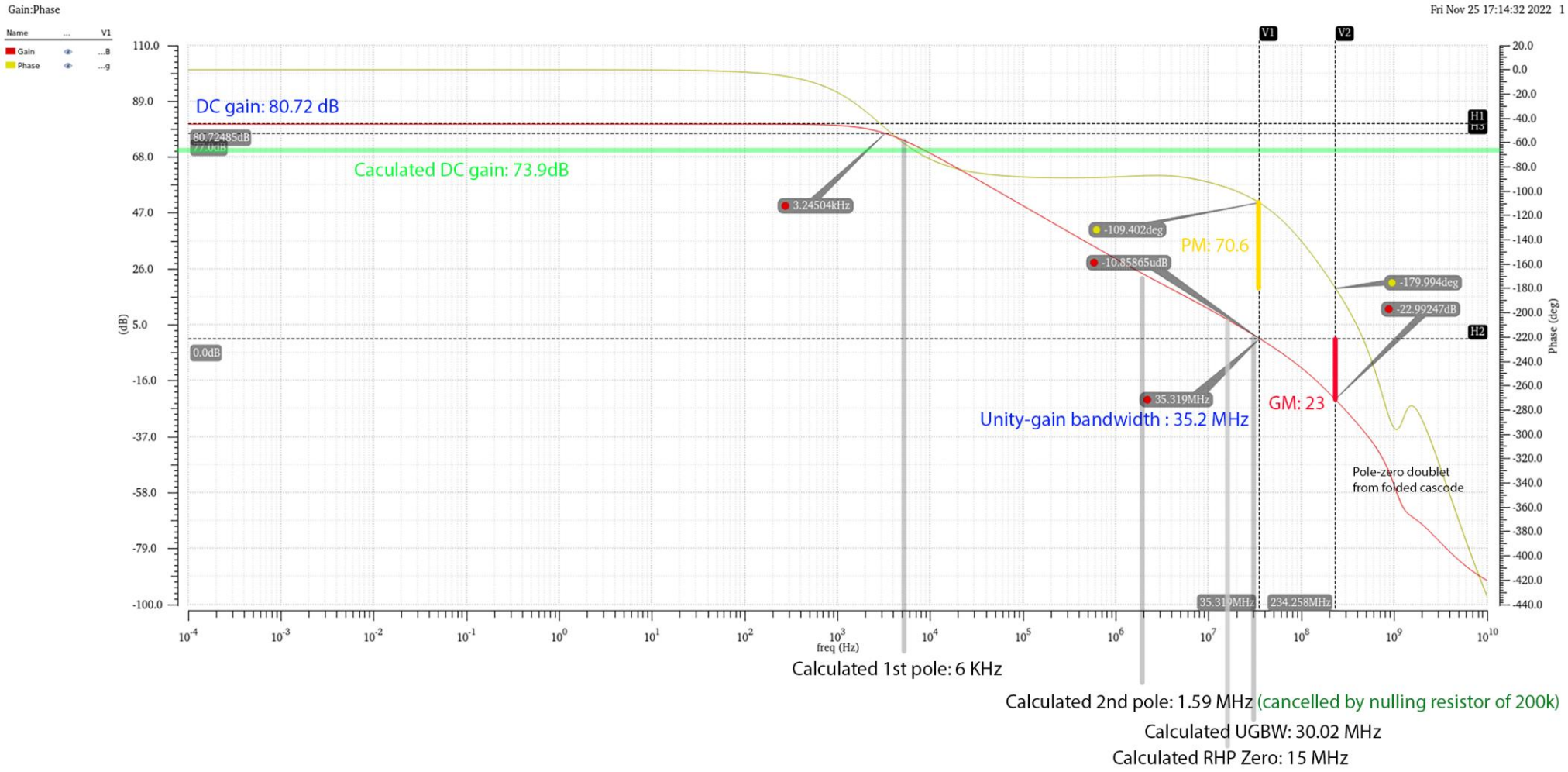
Parameter	Calculated	Simulated
IDBias	10u	13.84u
gmBias	100u	115.3u
CS ID	10u	43.67u
Power	0.198m	0.373m
Vov	0.20	0.205
DC gain	73.90	80.72dB
UGBW	30M	35.2MHz
fp1	6k	3.25k
fp2	1.59M	9M
fz	30M	200M
Cc	530f	530f
Rc	200k	86k
Vb2	0.70	0.604
Vb6	1.00	1.121
Rbias	10k	8k

Changes in R_c and common-source bias current has to do with the last design stage of margin optimization, namely UGBW was initially not met so g_{m9} had to be increased via more bias current; C_c was not decreased as it would move the poles closer, degrading phase margin. Once I had reasonable UGBW with an increase in g_{m9}, R_c was swept and the maxima of margins was picked, resulting in R_c = 86k. An increase in CS current – along with slight increase in I_{DBias} in general because of a smaller R_{Bias} - trivially increases current draw, increasing power.

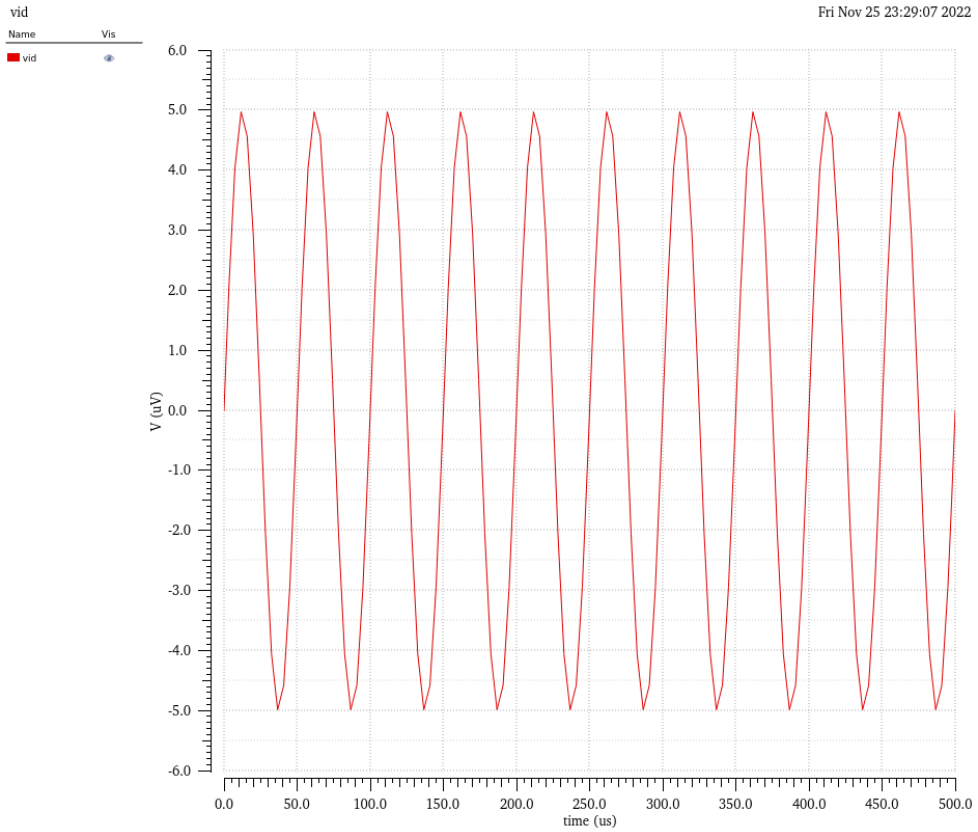
Interestingly, the reason why R_c change is likely of the discrepancy in the second non-dominant pole. My calculations totally neglected any intrinsic capacitances, only using the dominant C_{Load}. However, it is clear that some parasitic capacitances are at play, moving the second pole out and correspondingly the cancelling pole created by R_c.

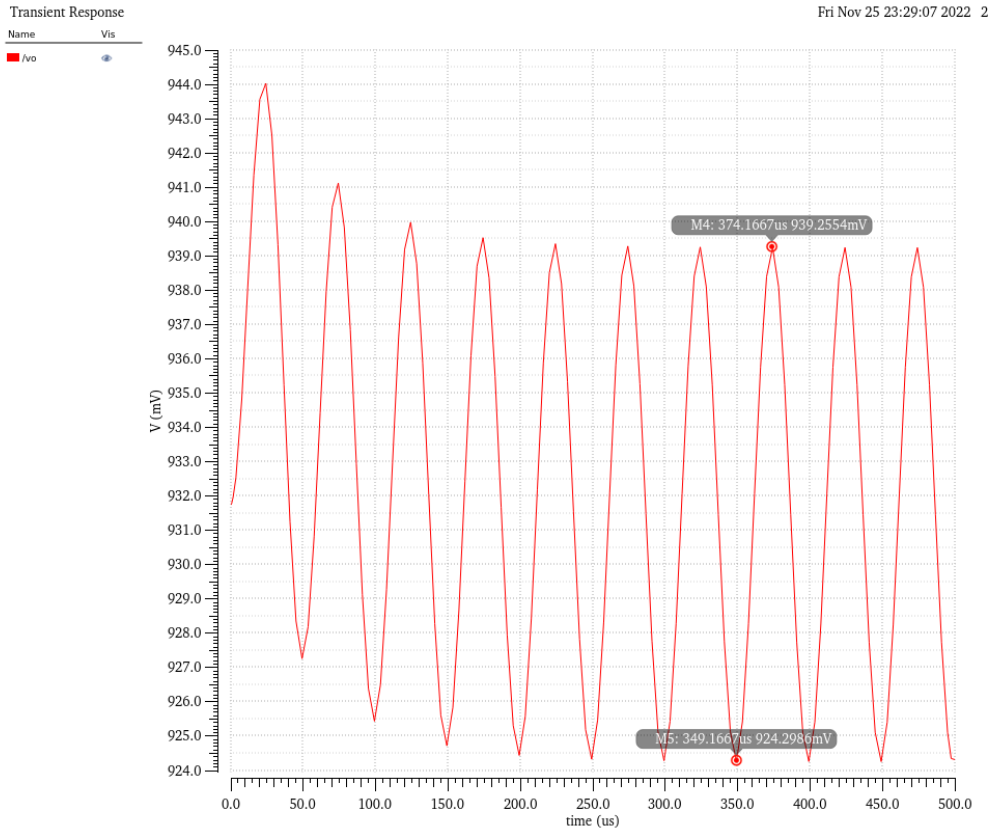
The RHP zero's move outward can be explained by the initial assumption of $g_{m9} = g_{mBias}$. This was not the case due to UGBW not being met and g_{m9} was increased as previously explained.

Simulation Bode Plot



Simulation Transient Plot





Comments and Conclusions

I had certainly underestimated this project, specifically the amount of time spent just trying to get a working design. Admittedly, I first approached the project with some SPICE monkeying but eventually learned, despite professor Hall's warning, that this brute force method leads to nothing. Even though hand calculations felt useless before doing them, the process converges to nominal values that are actually within the ballpark of an optimal simulation solution. This is the most valuable lesson I've taken from this project: when dealing with problems of many knobs to tweak, hand calculations provide a sanity check. Additionally, it also helps to arbitrarily, but also reasonably, pick some values for certain variables as it will greatly simplify the problem.

I could have definitely achieved better power consumption, namely by not overachieving the gain, but because of time constraints it proved unmanageable.

Seeing simulation DC operating points of the devices incrementally change as I tweaked parameters gave me immense intuition on how these devices work individually and as a whole system. It definitely illustrated the analogy of "balancing on a ball" when it came to biasing – this is due to how coupled everything is and changing one parameter has a higher order domino effect.

Overall, the project was my first shot at designing an IC architecture that would be more akin to industry standards, and it is the intuition of how one can break up an ostensibly complex IC architecture to decoupled modules that I value the most.